One or two P channel type MOSFETs (PchMOS) and one or two N channel type MOSFETs (NchMOS) are formed in their corresponding cell frames. Although the invention is not restricted in particular, the P channel type MOSFETs are placed on the upper side with the direction of each cell indicated by the character F as the reference, whereas the N channel type MOSFETs are similarly placed on the lower side. In the drawing, gate electrodes are respectively indicated by individual thick lines, and diffusion layers are formed so as to interpose the gate electrodes interposed therebetween, whereby they are formed as source and drain regions. The relationship between the direction of such a cell and the placement of the P channel type MOSFETs (PchMOS) and N channel type MOSFETs (NchMOS) is similar to the following in all embodiments.

On Page 10, please replace the first full paragraph with that of the following:

The sources and drains of the N channel type MOSFETs or the sources or drains of the parallel-configured P channel type MOSFETs can be electrically connected to one another without the special interconnections M1 by forming diffusion layers in common as in the case of the connections between the gate electrodes. In order to clearly represent the MOSFETs constituting the cells in the same drawing, the respective MOSFETs are represented so that the sources and drains are respectively formed with the gate electrodes interposed therebetween.

On Page 10, please replace the paragraph beginning in the last line thereof and bridging to page 11, line 8, with that of the following:

The cells employed in the present embodiment represent those supplied with at least one input signal from other than the cells. In other words, a circuit in which signal transfer routes are formed by a plurality of logic gate circuits alone, even of circuits constructed of a plurality of logic gates as in a flip-flop circuit, a counter circuit and a comparator or the like as described above, more specifically, logic circuits constructed by only an electrical connection which shares the use of the diffusion layers for the source and drain, and an electrical connection based on the wiring layer M1 corresponding to the first layer, can be regarded as one cell regardless of the size of the circuit scale.

On Page 12, please replace the second paragraph with that of the following:

The layout design of each random/logic circuit is performed as follows. After its circuit design, such a circuit is broken down into cells, which in turn are laid out and placed, and the design of wiring between the cells can be automatically performed by a computer. However, when the number of interconnections provided in the central portion of the cell sequence is insufficient, the interconnections remain non-wired or a short circuit in other interconnections is developed. Accordingly, the conventional circuit layout technology needs to re-layout the design of the cells in which wiring errors occur. However, the construction in which the slit cells are provided in the respective cells, as in the present embodiment, makes it possible to perform

automatic wiring which selects such slit cells and is performed in combination with the wiring channels provided outside the cell sequence upon the occurrence of a shortage of input signal routes in the automatic wiring design, owing to the inputting of information that the wiring routes based on such slit cells exist.

On Page 19, please replace the last paragraph beginning in the penultimate line and bridging to page 20, line 13, with that of the following:

As a premise condition for using the source line in common, the cell pitch and the pitch of each contact CONT of a power supply portion are set to be identical to each other. Here, the cell pitch corresponds to the minimum pitch of each interconnection employed in the semiconductor integrated circuit. Upon automatic wiring, interconnections corresponding to second and third layers are formed according to the pitch referred to above. When the two cell sequences are placed back to back and the source line is used in common, the condition that the pitch of each contact is matched with the cell pitch, is additionally set. As a result, the contact CONT and each through hole TH provided on the source line shared between the two cell sequences placed back to back can be matched with each other. Here, the contact CONT indicates a portion for connecting diffusion layers for the source and drain and a diffusion layer for an ohmic contact formed in a well, and a metal wiring layer M1 corresponding to a first layer. The through hole indicates a portion for connecting the metal wiring layer M1, corresponding to the first layer, and a metal wiring layer M2, corresponding to a second layer, to each other.

On Page 20, please replace the first full paragraph thereof with that of the following:

When each of the diffusion layers formed on the left side with a gate electrode of each N channel type MOSFET interposed therebetween is set as the source, each power-supply cell comprised of the contact CONT and the through hole TH provided in association with the above-described cell pitch is formed in a diffusion layer corresponding to the source and a P-type well region. A region corresponding to the drain is defined as a wiring region. Output interconnections each based on the metal wiring layer M1 corresponding to the first layer connected to the wiring channel (M2) formed outside along the cell sequence, for example, are formed in such a wiring region.

On Page 22, please replace the second full paragraph thereof with that of the following:

Figs. 9A and 9B are diagrams schematically illustrating a configuration of another embodiment of a dynamic RAM to which the present invention is applied. In the drawings, a schematic layout of diffusion layers is shown in Fig. 9A, and a schematic layout of wiring layers is illustrated in Fig. 9B. In the layouts shown in the drawings, typical portions of respective circuit blocks constituting the dynamic RAM are illustrated so that their principal parts are understood. They are formed over a single semiconductor substrate, such as monocrystal silicon, by a known semiconductor integrated circuit manufacturing technology.

On Page 23, please replace the first full paragraph thereof with that of the following:

In the present embodiment, a diffusion layer for forming a stabilized capacitance is formed in the central portion of the semiconductor chip, where the wiring channel corresponding to the third layer and the wiring channel corresponding to the second layer intersect. Although the invention is not restricted in particular, the stabilized capacitance is used as stabilized capacitance of each de-boosting power circuit for producing operating voltages for the peripheral circuits. The de-boosting power circuits are constructed as follows. As will be described later, a plurality of circuits are placed so as to be distributed to a portion where peripheral circuits lying in the longitudinally-extending central portion on the semiconductor chip are formed. Further stabilized capacitance or capacitors having small capacitance values are also connected by utilizing spatial semiconductor regions of the peripheral circuits. Since such distributedly-provided stabilized capacitance or capacitors make use of the semiconductor regions limited as described above, they are set to a small capacitance value as compared with the stabilized capacitance formed in the chip's central portion.